



PTO/SB/08a/b (08-03)

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Substitute for form 1449A/B/PTO				Complete If Known	
				Application Number	10/814,603-Conf. #5472
				Filing Date	March 31, 2004
				First Named Inventor	Shinsaku Higashi, et al
				Art Unit	2123
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	02008/105002

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)			
JO	BA	WO-2004/090562-A1	10-21-2004	Advantest Corporation	
JO	BB	JP-6-160482	06-07-1994		

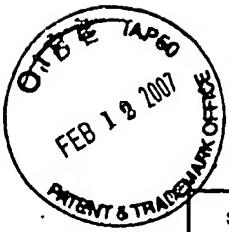
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
JO	CA	Patent Abstracts of Japan, Publication No. 06-160482, Dated 07-06-1994, 2 pages			
JO	CB	International Search Report, Int'l Appl. No. PCT/JP2004/004527, dated 07-01-2004, 1 page			

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PTO/SB/08A/B (09-06)

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Substitute for form 1449/PTO				Complete If Known	
				Application Number	10/814,603-Conf. #5472
				Filing Date	March 31, 2004
				First Named Inventor	Shinsaku Higashi
				Art Unit	2123
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	02008/105002

U.S. PATENT DOCUMENTS					
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ZD	AA*	US-6,028,439	02-22-2000	Arkin et al.	
ZD	AB*	US-5,931,953	08-03-1999	Lesmeister	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear T ⁶

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	CA	Supplementary European Search Report issued in European Application No. EP 04 72 3013 mailed on November 21, 2006, 3 pages			

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JO	AA*	US-6,026,230	02/2000	Lin et al.	
	AB*	US-5,841,967	11/1998	Sample et al.	
	AC*	US-6,009,256	12/1999	Tseng et al.	
	AD	US-2001/016922 A1	06-23-2001	Takesugi et al.	

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					T ⁶

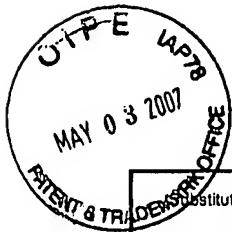
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JO	CA	U.S. Office Action issued for U.S. Application No. 10/404,002 mailed on February 22, 2006, 13 pages			
JO	CB	Sunburst-Design.com. "Sunburst Design - Introduction to Verilog-2001 Design", http://www.sunburst-design.com/verilog_training/Intro_Verilog_Training.pdf . 2/2003			
JO	CC	Donna Mitchell, "Manual and Automatic VHDL/Verilog Test Bench Coding Techniques", 2001, http://www.omimo.be/magazine/01q2_p027.pdf			
JO	CD	Supplementary European Search Report issued for EP 04 72 4396 mailed on March 31, 2006, 3 pages			
JO	CE	Xia J.Q. et al: "Dynamic Test Emulation for EDA-Based Mixed-Signal Test Development Automation" Proceedings of The International Test Conference (ITC). Washington, Oct. 21-25, 1995 (1995-10-21), pages 761-770, XP000552879 ISBN: 0-7803-2992-9			

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Used in Lieu of PTO/SB/08A/B
(Based on PTO 04-07 version)

Institute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete If Known	
				Application Number	10/814,603-Conf. #5472
				Filing Date	March 31, 2004
				First Named Inventor	Shinsaku Higashi
				Art Unit	2123
				Examiner Name	M. C. Jacob
Sheet	1	of	2	Attorney Docket Number	02008/105002

U.S. PATENT DOCUMENTS					
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		Number-Kind Code ² (# known)			
JO	AA*	US-2001/016922-A1	08-23-2001	Takasugi et al.	
JO	AB*	US-5,425,036	06-13-1995	Liu et al.	
JO	AC*	US-5,991,907	11-23-1999	Stroud et al.	
JO	AD*	US-6,077,304	06-20-2000	Kasuya	
JO	AE*	US-6,108,806	08-22-2000	Abramovici et al.	
JO	AF*	US-6,202,182	03-13-2001	Abramovici et al.	
JO	AG*	US-2002/0038203-A1	03-28-2002	Tsuchiya	
JO	AH*	US-6,631,487	10-07-2003	Abramovici et al.	
JO	AI*	US-2003/0005375-A1	01-02-2003	Takasugi et al.	

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		Country Code ³ -Number-Kind Code ⁴ (# known)			
JO	BA	JP-2000-267881	09-29-2000	Advantest Corp.	
JO	BB	JP-2002-141414	05-17-2002	Koninkl Philips Electronics NV	
JO	BC	JP-2001-522049	11-13-2001	Credence Systems Corp.	
JO	BD	JP-2001-506367	05-15-2001	Simd Solutions Inc.	
JO	BE	JP-2001-320386	11-16-2001	Nippon Electric Co.	
JO	BF	JP-2000-163456	06-16-2000	Hitachi Ltd.	

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JO	CA	Xia J.Q. et al: "Dynamic Test Emulation for EDA-Based Mixed-Signal Test Development Automation" Proceedings of The International Test Conference (ITC). Washington, Oct. 21-25, 1995, New York, IEEE, US, 21 October 1995 (1995-10-21), pages 761-770, XP000552879 ISBN: 0-7803-2992-9			
JO	CB	Explanation of Circumstances Relating To Accelerated Examination submitted in Japanese Application No. 2004-380598 dated March 1, 2007 and English translation thereof, 8 pages			
JO	CC	European Search Report issued in European Application No. EP 06 07 7162 dated February 23, 2007, 6 pages			
JO	CD	Castelnuovo A. et al: "Emulation-based Design Errors Identification" Defect and Fault Tolerance in VLSI Systems, 2002, DFT 2002. Proceedings. 17th IEEE International Symposium on 6-8 Nov. 2002, Piscataway, NJ, USA, IEEE, 6 November 2002 (2002-11-06), pages 365-371, XP010625026 ISBN: 0-7695-1831-1			
JO	CE	Japanese Office Action "Notification of Reasons for Rejection" issued in Japanese Application No. 2004-380598 mailed on April 3, 2007 and English translation thereof, 7 pages			

Examiner Signature	<i>JO</i>	Date Considered	6/14/07
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Substitute for form 1449/PTO				Complete If Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					
(Use as many sheets as necessary)					
Sheet	2	of	2		
Application Number	10/814,603-Conf. #5472				
Filing Date	March 31, 2004				
First Named Inventor	Shinsaku Higashi				
Art Unit	2123				
Examiner Name	M. C. Jacob				
Attorney Docket Number	02008/105002				

JO	CF	Dearborn, W.R., Perkins, E.G., Wong, J.J., Rolince, D., The Virtual Test program (VTest), AUTOTESTCON '98. IEEE Systems Readiness Technology Conference, 1998 IEEE, USA, August 27, 1998, pp. 149-159	
JO	CG	U.S. Office Action issued in U.S. Application No. 10/404,002 mailed on April 9, 2007, 16 pages	

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				Art Unit	2123
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		Number-Kind Code ² (if known)			
JO	AA	US-5,951,704	09-14-1999	Sauer et al.	(same as BA)
	AB	US-6,487,700	11-26-2002	Fukushima	(same as BB)
	AC	US-US2002/0193980 A1	12-19-2002	Higashi et al.	(same as BE)

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JO	BA	JP-10-320229	12-04-1998		(same as AA)
JO	BB	JP-2000-267881	09-29-2000		(same as AB)
JO	BC	JP-2001-51025	02-23-2001		
JO	BD	JP-2001-134457	05-18-2001		
JO	BE	JP-2002-333469	11-22-2002		(same as AC)

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JO	CA	Patent Abstracts of Japan, Publication No. 2001-051025 dated February 23, 2001, with full translation, 11 pages			✓
JO	CB	Patent Abstracts of Japan, Publication No. 2001-134457 dated May 18, 2001, with full translation, 12 pages			✓

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77285			